AF IFW

Docket No.: 49657-744

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Hiroshi MAKINO	:	Confirmation Number: 3244
Serial No.: 09/615,070	:	Group Art Unit: 2112
Filed: July 12, 2000	:	Examiner: Paul R. Meyers

For: BI-DIRECTIONAL BUS CIRCUITRY EXECUTING BI-DIRECTIONAL DATA TRANSMISSION WHILE AVOIDING FLOATING STATE

Mail Stop Appeal Brief - Patent
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Transmitted herewith is an Appeal Brief in the above-identified application.

☐ No additional fee is required.
☐ Applicant is entitled to small entity status under 37 CFR 1.27
☐ Also attached:

The fee has been calculated as shown below:

	NO. OF CLAIMS	HIGHEST PREVIOUSLY PAID FOR	EXTRA CLAIMS	RATE	FEE
Total Claims	13	20	0	$18.00 =	$0.00
Independent Claims	2	3	0	$86.00 =	$0.00
		Multiple claims newly presented			$0.00
		Fee for extension of time			$0.00
		Appeal Brief			$330.00
				Total of Above Calculations	$330.00

☒ Please charge my Deposit Account No. 500417 in the amount of $330.00. An additional copy of this transmittal sheet is submitted herewith.

☒ The Commissioner is hereby authorized to charge payment of any fees associated with this communication or credit any overpayment, to Deposit Account No. 500417, including any filing fees under 37 CFR 1.16 for presentation of extra claims and any patent application processing fees under 37 CFR 1.17.

Respectfully submitted,

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Date: July 27, 2004

WDC99 954080-1.049657.0744

Docket No.: 49657-744 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

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Hiroshi MAKINO	:	Confirmation Number: 3244
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For: BI-DIRECTIONAL BUS CIRCUITRY EXECUTING BI-DIRECTIONAL DATA TRANSMISSION WHILE AVOIDING FLOATING STATE

TRANSMITTAL OF APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

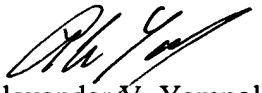
Sir:

Submitted herewith in triplicate is Appellant(s) Appeal Brief in support of the Notice of Appeal filed June 9, 2004. Please charge the Appeal Brief fee of $330.00 to Deposit Account 500417.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT WILL & EMERY LLP



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Docket No.: 49657-744 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
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For: BI-DIRECTIONAL BUS CIRCUITRY EXECUTING BI-DIRECTIONAL DATA TRANSMISSION WHILE AVOIDING FLOATING STATE

APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Appeal Brief is submitted in support of the Notice of Appeal filed June 9, 2004.

I. REAL PARTY IN INTEREST

The real party in interest is Renesas Technology Corporation, the assignee of the entire right, title and interest in and to the above-identified U. S. Application.

II. RELATED APPEALS AND INTERFERENCES

No other appeals or interferences are known to the Appellant, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-13 are pending. These claims stand under final rejection, from which rejection this appeal is taken.

IV. STATUS OF AMENDMENTS

The application has not been amended after final Office Action.

V. SUMMARY OF INVENTION

The application relates to a bi-directional bus circuitry for a semiconductor device, such as a microprocessor. In a mono-directional bus, the speed of transmission may be improved by including in a bus line, a repeater circuit operating as a signal buffer. However, in a bi-directional bus, repeaters must enable bi-directional signal amplification. Therefore, an arbiter circuit is required to control direction of signal transmission in each repeater.

FIG. 9 of the application shows a conventional bi-directional bus circuitry 500 that transmits data among four circuit blocks 10-a to 10-d over a data bus divided into bus nodes Nb1 and Nb2. A

repeater circuit 50 is connected between bus nodes Nb1 and Nb2. An arbiter circuit 520 selects a circuit block to/from which data is to be input/output and controls direction of signal transmission of the repeater circuit 50.

As described on page 3 of the specification, when the data bus in FIG. 9 is unused, i.e. when none of the circuit blocks 10-a to 10-d uses the data bus, repeater control signals CRP1 and CRP2 are inactivated. As a result, both bus nodes Nb1 and Nb2 go into a floating state (with unfixed potential level) resulting in a possibility of circuit breakdown in the input and output buffers of the circuit blocks connected to the bus node.

FIG. 10 of the application shows a conventional mono-directional bus, in which the problem of unfixed data bus potential level is solved using a bus circuitry 600 that enables the bus potential to be fixed when the bus is not used. The bus circuitry 600 includes n tristate buffers GT1 to GTn corresponding to data D1 to Dn, respectively, and a bus line BUS connected to an output node of each tristate buffer.

As described on page 4 of the specification, even when all tristate buffers are set to a high-impedance state and bus line BUS is not used, it is possible to fix the potential level of bus line BUS at a prescribed potential level. Therefore, problems resulting from the unfixed potential level of the bus line BUS can be avoided. However, as stressed on page 4 of the specification, it is difficult to apply the technique for fixing the bus potential used in a mono-directional bus shown in FIG. 10, directly to a bi-directional bus circuitry.

The present invention provides a configuration of a bi-directional bus circuitry capable of preventing potential level of an unused data bus from being unfixed. As claimed in claim 1, shown, for example, in FIG. 2 and described on pages 10-11 of the specification, a bi-directional circuitry 100 in accordance with one aspect of the present invention includes a data bus for bi-directional transferring

data among circuit blocks 10a to 10d. The data bus is divided into bus nodes Nb1 and Nb2 by a repeater circuit 50 for bi-directional signal transmission between bus nodes Nb1 and Nb2. A bus potential fixing circuit 60 is provided for fixing the potential level of bus node Nb1 when the data bus is not used. An arbiter circuit 20 controls the operations of the repeater circuit 50 and bus potential fixing circuit 60. The repeater circuit 50 includes a tristate buffer 51 for amplifying and transmitting a signal in the direction from the bus node Nb1 to the bus node Nb2, and a tristate buffer 52 for amplifying and transmitting a signal in the direction from the bus node Nb2 to the bus node Nb1.

As described on pages 12-14, the arbiter circuit 20 generates repeater control signals CRP1 and CRP2, and a bus potential fixing signal CBF. When the data bus is not used, the bus potential fixing circuit 60 is controlled by the bus potential fixing signal CBF to set a potential level of the bus node Nb1 at a ground potential. Further, when the data bus is not used, the repeater control signal CRP1 is activated and the repeater control signal CRP2 is inactivated to respectively activate and inactivate the tristate buffers 51 and 52. As a result, the potential level of the bus node Nb1 is transmitted to the bus node Nb2. Such a configuration makes it possible to set the potential levels of the both bus nodes Nb1 and Nb2 to the ground potential when the data bus is not used.

As claimed in independent claim 10, shown, for example, in FIG. 7 and described on pages 20-21, in accordance with another aspect of the invention, a bi-directional bus circuitry 300 including an arbiter circuit 320 may be provided without a potential fixing circuit. The arbiter circuit 320 generates repeater control signals CRP1 and CRP2. In particular, when neither circuit block 10-c nor circuit block 10-d is used, the repeater control signal CR1 is activated. When neither circuit block 10-a nor circuit block 10-b is used, the repeater control signal CRP2 is activated. When the data bus is not used, arbiter circuit 320 activates both repeater control signals CRP1 and CRP2, and, therefore, both tristate buffers 51 and 52 of the repeater circuit 50 are activated and amplify data. Such a configuration makes

it possible to set the potential level of each bus node either to a power supply potential level or to a ground potential level when the data bus is not used.

As explained on pages 20 and 21, the bi-directional bus circuitry 300 provides effects similar to the effects provided by the bi-directional bus circuitry 100 at a smaller area.

VI. ISSUES

Whether claims 1-13 are unpatentable over Applicant's Admitted Prior Art (combination of FIGS. 9 and 10) under 35 U.S.C. § 103(a).

VII. GROUPING OF CLAIMS

Appellant submits that the claims of the rejected group do not stand or fall together. The claims being considered to be separately patentable for the reasons presented in the Argument section of this Brief.

VIII. THE ARGUMENT

To establish a *prima facie* case of obviousness under 35 U.S.C. § 103, two basic criteria must be met. First, there must be some suggestion or motivation in the references themselves to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success for the modification or combination of references. The teaching or suggestion to make the modification or combination of prior art and the reasonable expectation of success must both be found in the prior art, and not based on Appellant 's disclosure. ***In re Vaeck***, 947 F.2d 488, 20 USPQ2d 1438

(Fed. Cir. 1991).

As demonstrated below, the Examiner's conclusion of obviousness is based on his inaccurate interpretation of the Appellant's disclosure rather than on the suggestion and the reasonable expectation of success found in the prior art.

Claim 1 recites a bi-directional bus circuitry shared among a plurality of circuit blocks. The bus circuitry comprises:

- a data bus divided into (J+1) (J: natural number being 1 or more than 1) bus nodes, each of the plurality of circuit blocks being connected to one of the (J+1) bus nodes;

- a potential fixing circuit provided corresponding to one of the (J + 1) bus nodes, for setting potential level of corresponding the bus node to a prescribed potential when data is input to/output from none of the plurality of circuit blocks;

- J repeater circuits provided between adjacent the bus nodes respectively, each repeater circuit having a first signal transmitting circuit transmitting data from one to the other of the adjacent bus nodes, and a second signal transmitting circuit transmitting data from the other to the one of the adjacent bus nodes; and

- an arbiter circuit receiving circuit block information for specifying a circuit block which is an object of data output, and controlling activation of the first and second signal transmitting circuits.

Claim 1 specifies that the arbiter circuit activates, when the data is input to/output from none of the plurality of circuit blocks, either one of the first and second signal transmitting circuits in each repeater circuit, so that potential level of the bus node corresponding to the potential fixing circuit is transmitted to the data bus entirely.

Independent claim 10 recites a bi-directional bus circuitry shared among a plurality of circuit blocks, comprising:

-a data bus divided into (J + 1) (J: natural number being 1 or more than 1) bus nodes, each of the plurality of circuit blocks being connected to one of said (J + 1) bus nodes;

-J repeater circuits arranged between adjacent said bus nodes, each of which includes a first signal transmitting circuit transmitting data from one to the other of the adjacent bus nodes, and a second signal transmitting circuit transmitting data from the other to the one of the adjacent bus nodes; and

-an arbiter circuit receiving circuit information for specifying a circuit block which is an object of data output, and controlling activation of the first and second signal transmitting circuits in each of the repeater circuits.

Claim 10 specifies that the arbiter circuit activates both of the first and second signal transmitting circuits in each of the repeater circuits when the data bus is not used, that is, when data is input to/output from none of the plurality of circuit blocks.

The Examiner considers the arrangement in FIG. 9 of the present application to differ from the claimed invention only in that FIG. 9 does not show the arbiter circuit activating, when the data is input to/output from none of the plurality of circuit blocks, either one of the first and second signal transmitting circuits in each repeater circuit, so that potential level of the bus node corresponding to the potential fixing circuit is transmitted to the data bus entirely. FIG. 10 is relied upon for showing this element.

The Examiner asserts that "[i]t would have been obvious...to apply AAPA figure 10 potential fixing circuit to all nodes of the repeater because this would have fixed the problem identified by AAPA figure 10 in the system of figure 9."

It is respectfully submitted that the Examiner's statement is inaccurate. The Appellant's disclosure on page 3, lines 15-33, indicates, in connection with the arrangement in FIG. 9, that "with

the potential level of the bus node being unfixed, the potential level of the bus node comes to be the intermediate potential, possibly causing a constant current, which will be consumed wastefully, in the input and output buffers of the circuit blocks which are connected to the bus node. If the potential of the bus node should be higher than a power supply potential, which corresponds to the H level potential of the data or lower than the ground potential which corresponds to the L level potential of the data because of a noise or the like, there is a possibility of circuit break down in the input and output buffers of the circuit blocks connected to the bus node. Japanese Patent Laying-Open No. 63-85852 proposes a solution to this problem of unfixed potential level of the data bus, which solution provides a bus circuitry configuration allowing fixing of the bus potential when the bus is not used. Fig. 10 is a schematic diagram of a conventional bus circuitry allowing fixing of the bus potential when not in use."

Accordingly, the arrangements in FIGS. 9 and 10 do not contain the teaching or suggestion to make the modification or combination of prior art suggested by the Examiner, and the reasonable expectation of success. It is only the Appellant's disclosure rather than the prior art identifies the problem of the arrangement in FIG. 9 and a possible solution.

However, the specification on page 4, lines 18-20 indicates that "it is difficult to apply the technique for fixing the bus potential when not in use shown in Fig. 10, directly to a bi-directional bus circuitry" (page 4, lines 18-20). It is noted that while FIG. 10 shows a mono-directional bus circuit, FIG. 9 shows bi-directional bus circuitry.

Accordingly, the Appellant's disclosure indicates that the arrangement in FIG. 10 is not a proper solution for the problem of the arrangement in FIG. 9.

It is noted that if the Examiner erroneously considers the Appellant's disclosure in the Background section of the present application to be prior art, he should realize that the Background

section expressly **teaches away** from modifying the arrangement in FIG. 9 by incorporating the arrangement in FIG. 10, thereby constituting further **evidence of nonobviousness**. ***In re Bell***, 991 F.2d 781, 26 USPQ2d 1529 (Fed. Cir. 1993); ***In re Hedges***, 783 F.2d 1038, 228 USPQ 685 (Fed. Cir. 1986); ***In re Marshall***, 578 F.2d 301, 198 USPQ 344 (CCPA 1978).

Moreover, as indicated above, the Examiner suggests applying "AAPA figure 10 potential fixing circuit to all nodes of the repeater..." However, one skilled in the art would realize that if the potential fixing circuit (transistor QTN of FIG. 10) for a mono-directional bus were provided for each of the divided bus nodes Nb1 and Nb2 in the bi-directional data bus shown in FIG. 9, it would result in reducing the data transmission rate on the data bus. More specifically, when the data bus is used, both transistors QTN respectively connected to the bus nodes Nb1 and Nb2 are turned off. Therefore, parasitic capacitance of drains in the transistors QTN increases the parasitic resistance of the data bus, reducing the data transmission rate.

It is well settled that if proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. ***In re Gordon***, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).

As discussed above, the modification suggested by the Examiner would render the bi-directional bus in FIG. 9 being modified unsatisfactory for its intended purpose, i.e. high-speed data transmission. Therefore, there is no suggestion or motivation to make the proposed modification.

It is noted that the Examiner states that "in lights of the current arguments," the rejection under 35 U.S.C. § 102 would be "more appropriate that the current examiners (sic) 35 U.S.C. 103 rejection." However, the Examiner concludes that the rejection under 35 U.S.C. § 102 would be inappropriate "since the AAPA teaches two different systems" (Office Action of March 19, 2004, the paragraph bridging pages 4 and 5).

Accordingly, the Examiner admits that the rejection under 35 U.S.C. § 102 is not appropriate, and the rejection under 35 U.S.C. § 103 is even less appropriate.

Moreover, as demonstrated below, even if the arrangement in FIG. 9 were modified in accordance with the Examiner's suggestion, the invention recited in claims 1 and 8 would not result.

In particular, the combined teachings of FIGS. 9 and 10 would not suggest that the arbiter circuit activates, when the data is input to/output from none of the plurality of circuit blocks, either one of the first and second signal transmitting circuits in each repeater circuit, so that potential level of the bus node corresponding to the potential fixing circuit is transmitted to the data bus entirely, as claim 1 recites.

More specifically, if the potential fixing circuit (transistor QTN of FIG. 10) were provided for each of the divided bus nodes Nb1 and Nb2 in the bi-directional data bus shown in FIG. 9, the arbiter circuit 520 (FIG. 9) would inactivate both tristate buffers 51 and 52 (corresponding to the first and second signal transmitting circuits of the repeater), when the data is not transferred among the circuit blocks.

Accordingly, the combined teachings of FIGS. 9 and 10 would not suggest activating either one of the first and second signal transmitting circuits, when the data is input to/output from none of the plurality of circuit blocks, as claim 1 recites.

Also, the combined teachings of FIGS. 9 and 10 would not suggest that the arbiter circuit activates both of the first and second signal transmitting circuits in each of the repeater circuits when the data bus is not used, that is, when data is input to/output from none of the plurality of circuit blocks, as independent claim 10 recites. It is noted that the Examiner has failed to address the limitations of the independent claim 10.

As discussed above, if the potential fixing circuit (transistor QTN of FIG. 10) were provided for

each of the divided bus nodes Nb1 and Nb2 in the bi-directional data bus shown in FIG. 9, both of the first and second signal transmitting circuits of the repeater would be inactivated (rather than activated, as claim 10 requires) when the data bus is not used.

It is well settled that the test for obviousness is what the combined teachings of the references would have suggested to those having ordinary skill in the art. ***Cable Electric Products, Inc. v. Genmark, Inc.***, 770 F.2d 1015, 226 USPQ 881 (Fed. Cir. 1985). In determining whether a case of prima facie obviousness exists, it is necessary to ascertain whether the prior art teachings appear to be sufficient to one of ordinary skill in the art to suggest making the claimed substitution or other modification. ***In re Lalu***, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1984).

As demonstrated above, the prior art teachings in FIGS, 9 and 10 are not sufficient to arrive at the inventions recited in claims 1 and 10.

Furthermore, the combined teachings of FIGS. 9 and 10 are not sufficient to suggest the features of claims 2-9 and 11-13 respectively dependent from claims 1 and 10.

For example, as demonstrated above, the combined teachings of FIGS. 9 and 10 would not teach or suggest:

-the arbiter circuit activating said first signal transmitting circuit when data is output from none of said circuit blocks belonging to said second circuit block group, and activating said second signal transmitting circuit when data is output from at least one of said circuit blocks belonging to said second circuit block group, as claim 3 requires;

-the potential fixing circuit including a switch circuit connected between a power supply node supplying a potential level corresponding to either one of said high level and said low level and said corresponding bus node, and turned on when the data bus is not used, as claim 4 requires;

-the arbiter circuit activating said first signal transmitting circuit when data is output from none

of said circuit blocks belonging to said second circuit block group, and activating said second signal transmitting circuit when data is not output from any of said circuit blocks belonging to said first circuit block group, as claim 12 recites;

-the arbiter circuit activating said first signal transmitting circuit in each repeater circuit when data is output from none of said circuit blocks belonging to said second circuit block group, and activating said second signal transmitting circuit in each repeater circuit when data is output from none of said circuit blocks belonging to said first circuit block group, as claim 13 recites.

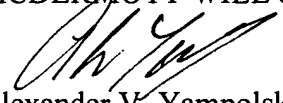
It is noted that inasmuch as claims 1-13 are separately patentable within the meaning of 35 U.S.C. 103, they do not stand or fall together.

IX. CONCLUSION

For the reasons advanced above, Appellant respectfully contends that the rejection of claims 1-13 as being obvious under 35 U.S.C. § 103 is improper as the Examiner has not met the burden of establishing a *prima facie* case of obviousness. Reversal of the rejections in this appeal is respectfully requested.

Respectfully submitted,

MCDERMOTT WILL & EMERY LLP



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Date: July 27, 2004

X. APPENDIX

1. A bi-directional bus circuitry shared among a plurality of circuit blocks, comprising:

a data bus divided into (J + 1) (J: natural number being 1 or more than 1) bus nodes,

each of said plurality of circuit blocks being connected to one of said (J + 1) bus nodes;

a potential fixing circuit provided corresponding to one of said (J + 1) bus nodes, for setting potential level of corresponding said bus node to a prescribed potential when data is input to/output from none of said plurality of circuit blocks;

J repeater circuits provided between adjacent said bus nodes respectively,

each repeater circuit having

a first signal transmitting circuit transmitting data from one to the other of said adjacent bus nodes, and

a second signal transmitting circuit transmitting data from said the other to said one of said adjacent bus nodes; and

an arbiter circuit receiving circuit block information for specifying a circuit block which is an object of data output, and controlling activation of said first and second signal transmitting circuits,

said arbiter circuit activating, when said data is input to/output from none of said plurality of circuit blocks, either one of said first and second signal transmitting circuits in each repeater circuit, so that potential level of said bus node corresponding to said potential fixing circuit is transmitted to said data bus entirely.

2. The bi-directional bus circuitry according to claim 1, wherein

said first signal transmitting circuit includes a first tristate buffer connected in a direction from

said one to said the other of said adjacent bus nodes and controlled by said arbiter circuit, and

said second signal transmitting circuit has a second tristate buffer connected in a direction from said the other to said one of said adjacent bus nodes and controlled by said arbiter circuit.

3. The bi-directional bus circuitry according to claim 1, wherein

J is 1;

said plurality of circuit blocks is divided into a first circuit block group connected to one of two bus nodes, and a second circuit block group connected to the other of said two bus nodes;

said potential fixing circuit is provided corresponding to either one of said two bus nodes;

said first signal transmitting circuit is provided for transmitting data from said one to said the other of said two bus nodes;

said second signal transmitting circuit is provided for transmitting data from said the other to said one of said two bus nodes; and

said arbiter circuit activates said first signal transmitting circuit when data is output from none of said circuit blocks belonging to said second circuit block group, and activates said second signal transmitting circuit when data is output from at least one of said circuit blocks belonging to said second circuit block group.

4. The bi-directional bus circuitry according to claim 1, wherein

data transmitted over said data bus has two states of high level and low level;

said potential fixing circuit includes a switch circuit connected between a power supply node supplying a potential level corresponding to either one of said high level and said low level and said corresponding bus node; and

said arbiter circuit turns on said switch circuit when said data bus is not used.

5. The bi-directional bus circuitry according to claim 4, wherein said power supply node supplies a potential level corresponding to said low level, and

said switch circuit has an N type field effect transistor.

6. The bi-directional bus circuitry according to claim 4, wherein

said power supply node supplies a potential level corresponding to said high level, and

said switch circuit has a P type field effect transistor.

7. The bi-directional bus circuitry according to claim 1, wherein

J is at least 2; and

said potential fixing circuit is provided corresponding to one of (J – 1) bus nodes among said (J + 1) bus nodes other than two bus nodes positioned at opposing ends.

8. The bi-directional bus circuitry according to claim 1, wherein

J is at least 2; and

said potential fixing circuit is provided corresponding to either one of two bus nodes positioned at opposing ends, among said (J + 1) bus nodes.

9. The bi-directional bus circuitry according to claim 8, wherein

said plurality of circuit blocks is divided into a first circuit block group connected to one of said two bus nodes positioned at the opposing ends and a second circuit block group connected to the other

of said two bus nodes positioned at the opposing end; and

said first and second signal transmitting circuits in each repeater circuit are controlled by first and second control signals which are common to said J repeater circuits.

10. A bi-directional bus circuitry shared among a plurality of circuit blocks, comprising:

a data bus divided into (J + 1) (J: natural number being 1 or more than 1) bus nodes,

each of said plurality of circuit blocks being connected to one of said (J + 1) bus nodes;

J repeater circuits arranged between adjacent said bus nodes,

each of said repeater circuits including

a first signal transmitting circuit transmitting data from one to the other of said adjacent bus nodes, and

a second signal transmitting circuit transmitting data from said the other to said one of said adjacent bus nodes; and

an arbiter circuit receiving circuit information for specifying a circuit block which is an object of data output, and controlling activation of said first and second signal transmitting circuits in each of said repeater circuits,

said arbiter circuit activating both of said first and second signal transmitting circuits in each of said repeater circuits when said data bus is not used, that is, when data is input to/output from none of said plurality of circuit blocks.

11. The bi-directional bus circuitry according to claim 10, wherein

said first signal transmitting circuit includes a first tristate buffer connected in a direction from said one to said the other of said adjacent bus nodes and controlled by said arbiter circuit, and

said second signal transmitting circuit has a second tristate buffer connected in a direction from said the other to said one of said adjacent bus nodes and controlled by said arbiter circuit.

12. The bi-directional bus circuitry according to claim 10, wherein

J is 1;

said plurality of circuit blocks is divided into a first circuit block group connected to one of two bus nodes, and a second circuit block group connected to the other of said two bus nodes;

said first signal transmitting circuit is provided for transmitting data from said one to said the other of said two bus nodes;

said second signal transmitting circuit is provided for transmitting data from said the other to said one of said two bus nodes; and

said arbiter circuit activates said first signal transmitting circuit when data is output from none of said circuit blocks belonging to said second circuit block group, and activates said second signal transmitting circuit when data is not output from any of said circuit blocks belonging to said first circuit block group.

13. The bi-directional bus circuitry according to claim 10, wherein

J is at least 2;

said plurality of circuit blocks is divided into a first circuit block group connected to one of two bus nodes positioned at opposing ends, and a second circuit block group connected to the other of said two bus nodes;

said first signal transmitting circuit in each repeater circuit is provided for transmitting data in a direction from said one to said the other of said two bus nodes;

said second signal transmitting circuit in each repeater circuit is provided for transmitting data in a direction from said the other to said one of said two bus nodes;

said first and second signal transmitting circuits in each repeater circuit are controlled by first and second control signals provided commonly to said J repeater circuits; and

said arbiter circuit activates said first signal transmitting circuit in each repeater circuit when data is output from none of said circuit blocks belonging to said second circuit block group, and activates said second signal transmitting circuit in each repeater circuit when data is output from none of said circuit blocks belonging to said first circuit block group.

Ap plicant: Hiroshi MAKINO Docket No. 49657-744

Title: BI-DIRECTIONAL BUS CIRCUITRY EXECUTING BI-DIRECTIONAL DATA TRANSMISSION WHILE AVOIDING FLOATING STATE

Serial/Reg./Patent No. 09/615,070

Date Sent: 7/27/2004 ☒ Hand Carried ☐ Fax ☐ Electronic ☐ Cert. of Mailing ☐ First Class Mail ☐ Express Mail No. _____

☐ Transmittal Letter

New Patent App ☐ Utility ☐ Design ☐ Cont. ☐ CIP ☐ Div. ☐ PCT ☐ RCE ☐ Prov

☐ Other: _____

_____ pages of Specification

_____ pages of Claims

_____ pages of Abstract

_____ pages of Formal/Informal Drawings

☐ Small Entity ☐ Large Entity

☐ Declaration/Power of Attorney

☐ Recordation of Assignment/Security Agreement

☐ Information Disclosure Statement

_____ Form PTO 1449

_____ copies of cited references

☐ Preliminary Amendment

☐ Response to Missing Parts Notice

☐ Resp. to Notice to Correct App. Papers

☐ Certified Copy of Priority Doc.

☐ Claim for Convention Priority

☒ Response/Amendment to Office Action of March 19, 2004

☐ Request for ___ month Extension of Time

☐ Letter submitting _____pages of drawings

☐ Req. for Approval of Drawing Amendments

☐ Req. for Oral Hearing

☐ Not. of Appeal ☒ Appeal Brief ☐ Reply Brief

☐ Rule 312 Amendment/Letter

☐ Req. for Acknowledgement of Cited Art

☐ Issue Fee

☐ Publication Fee

☐ Req. for Certificate of Correction

☐ Maintenance Fee for _____years after grant

☐ Fee Address Indication Form _____

☐ Terminal Disclaimer

☐ Petition to Commissioner

☐ Status Inquiry

☐ Other ____

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Ap plicant: Hiroshi MAKINO Docket No. 49657-744

Title: BI-DIRECTIONAL BUS CIRCUITRY EXECUTING BI-DIRECTIONAL DATA TRANSMISSION WHILE AVOIDING FLOATING STATE

Serial/Reg./Patent No. 09/615,070

Date Sent: 7/27/2004 ☒ Hand Carried ☐ Fax ☐ Electronic ☐ Cert. of Mailing ☐ First Class Mail ☐ Express Mail No. _____

☐ Transmittal Letter

New Patent App ☐ Utility ☐ Design ☐ Cont. ☐ CIP ☐ Div. ☐ PCT ☐ RCE ☐ Prov

☐ Other: _____

_____ pages of Specification

_____ pages of Claims

_____ pages of Abstract

_____ pages of Formal/Informal Drawings

☐ Small Entity ☐ Large Entity

☐ Declaration/Power of Attorney

☐ Recordation of Assignment/Security Agreement

☐ Information Disclosure Statement

_____ Form PTO 1449

_____ copies of cited references

☐ Preliminary Amendment

☐ Response to Missing Parts Notice

☐ Resp. to Notice to Correct App. Papers

☐ Certified Copy of Priority Doc.

☐ Claim for Convention Priority

☒ Response/Amendment to Office Action of March 19, 2004

☐ Request for ___ month Extension of Time

☐ Letter submitting _____pages of drawings

☐ Req. for Approval of Drawing Amendments

☐ Req. for Oral Hearing

☐ Not. of Appeal ☒ Appeal Brief ☐ Reply Brief

☐ Rule 312 Amendment/Letter

☐ Req. for Acknowledgement of Cited Art

☐ Issue Fee

☐ Publication Fee

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